ABSTRACT OF THE DISCLOSURE

A clock control circuit for reducing jitter has at least one averaging circuit for generating, and outputting from an output terminal, a signal having a time difference obtained by internally dividing a time difference between first and second signals input respectively from first and second input terminals. First and second clock signals are supplied respectively to the first and second input terminals of the timing averaging circuit, and a clock in which a time difference between pulses of the first and second clock signals is averaged is generated.